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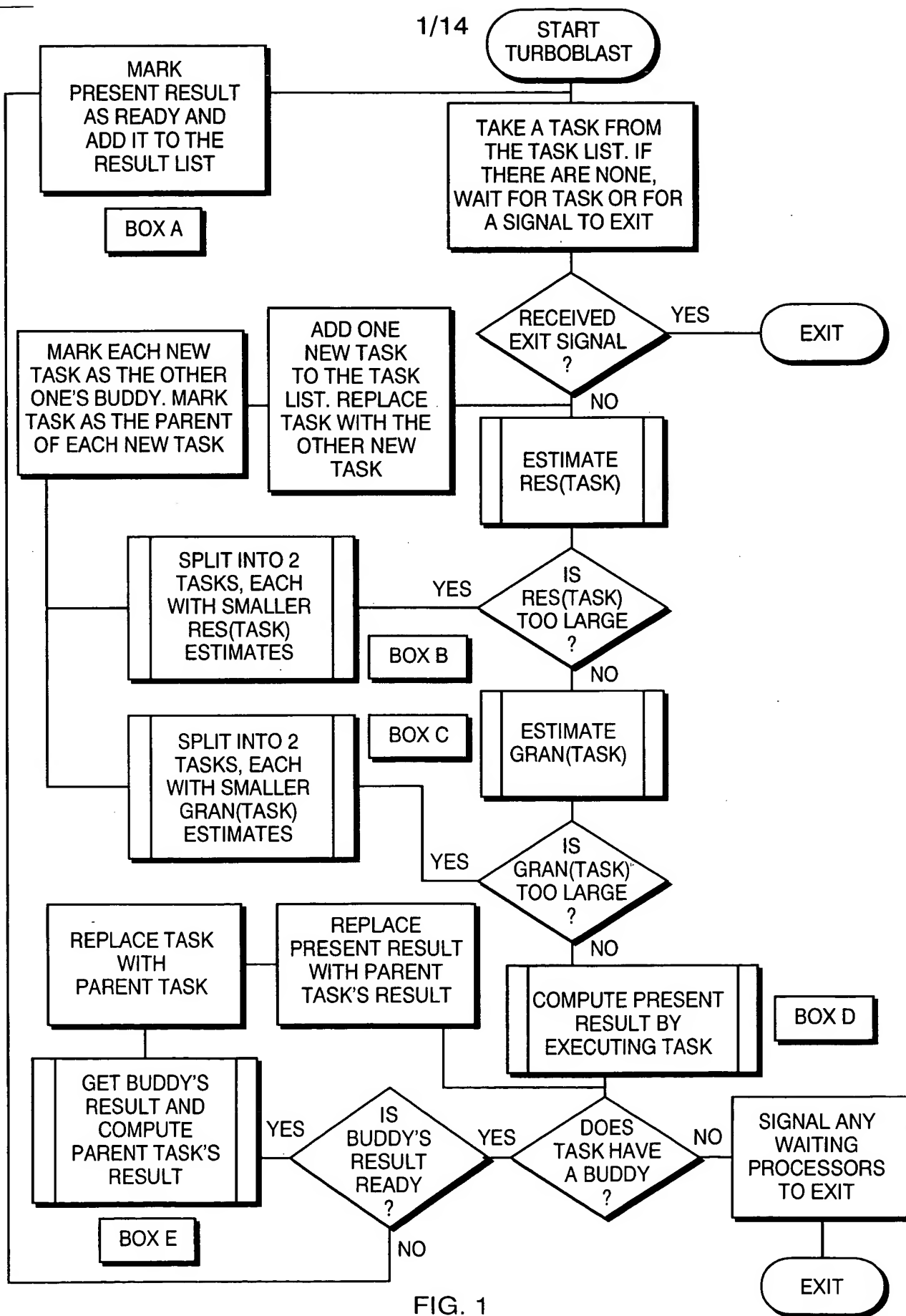


FIG. 1

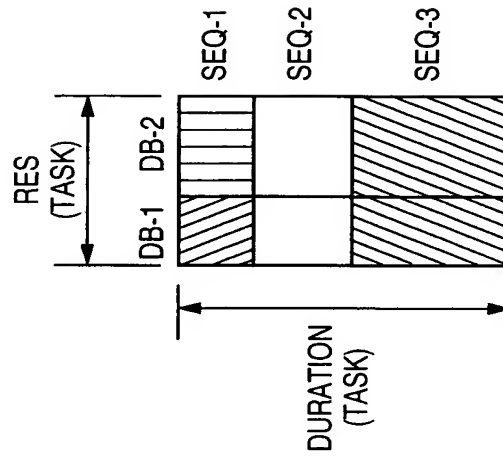


FIG. 2B

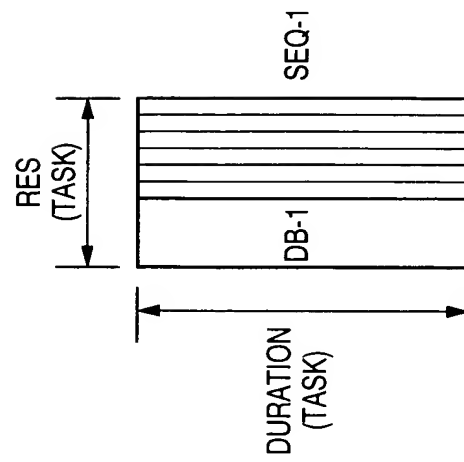
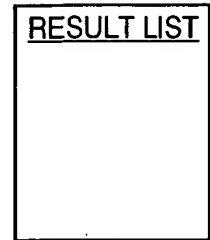
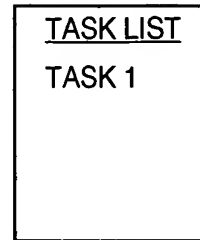
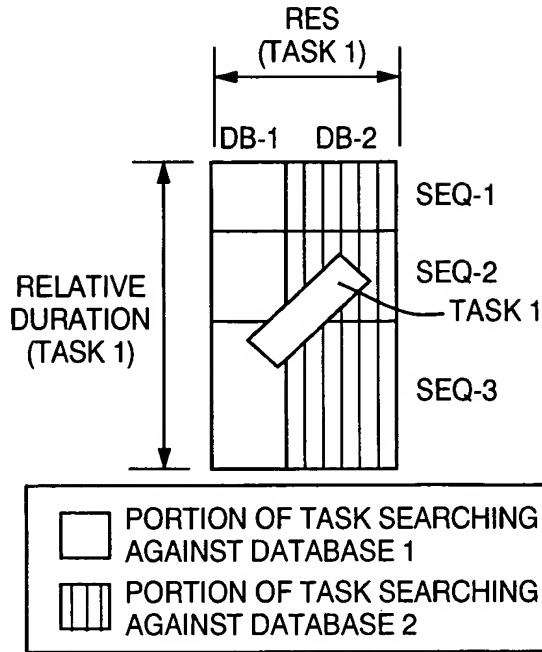


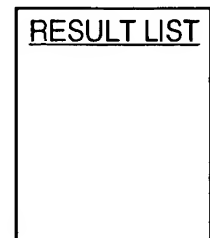
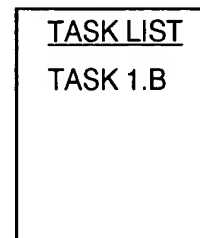
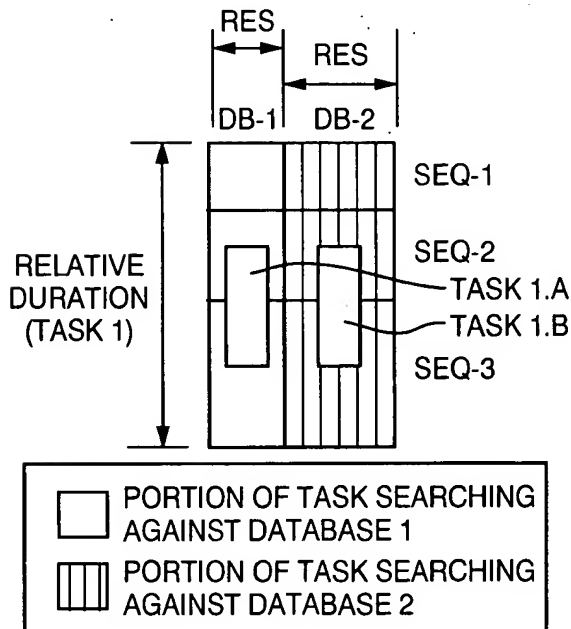
FIG. 2A





PROCESSOR 1: CURRENTLY IDLE  
PROCESSOR 2: CURRENTLY IDLE

FIG. 3A



PROCESSOR 1: DONE DIVIDING TASK 1.B.  
ABOUT TO WORK ON TASK 1.A  
PROCESSOR 2: CURRENTLY IDLE. ABOUT  
TO WORK ON TASK 1.B

FIG. 3B

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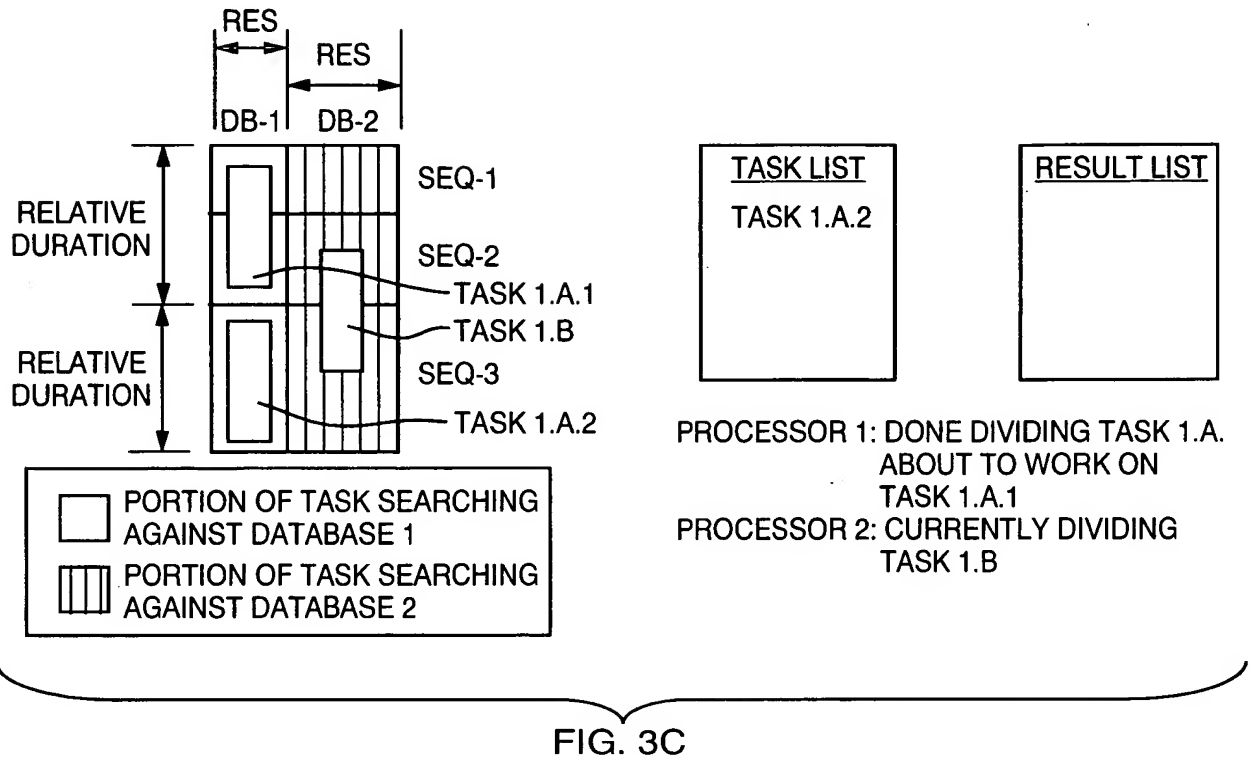


FIG. 3C

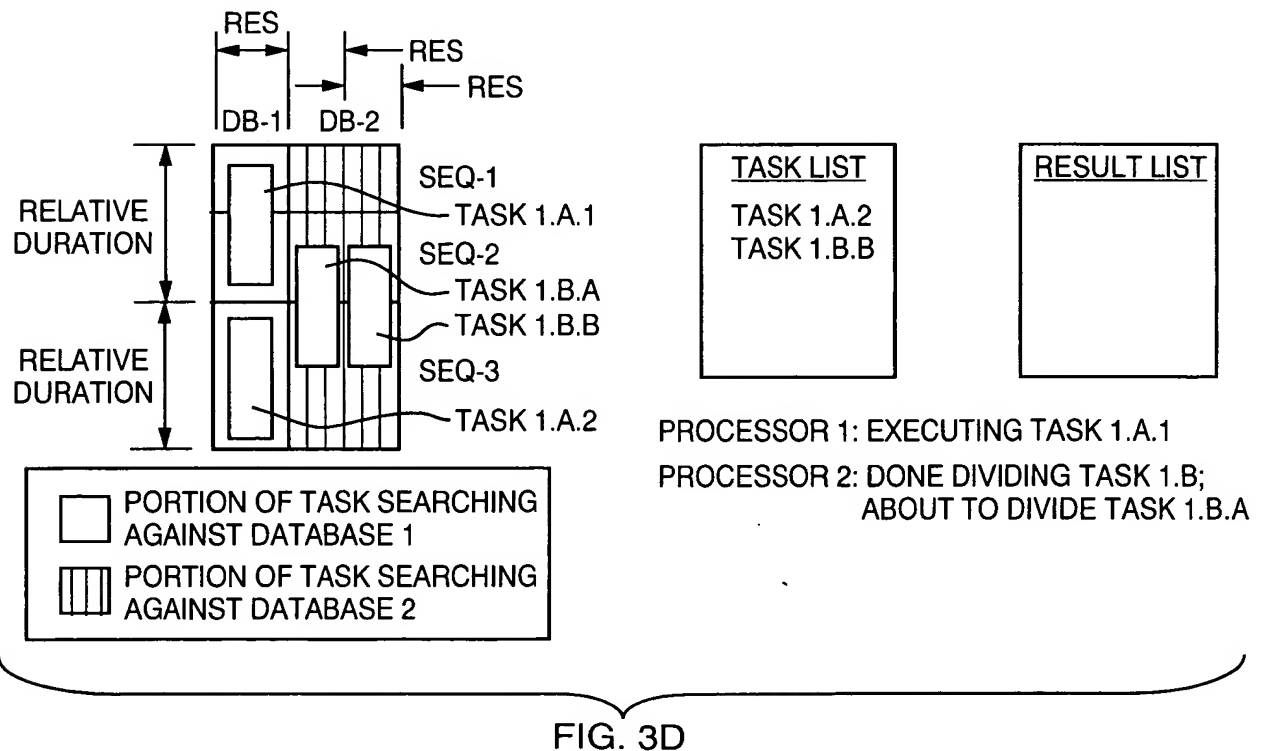


FIG. 3D

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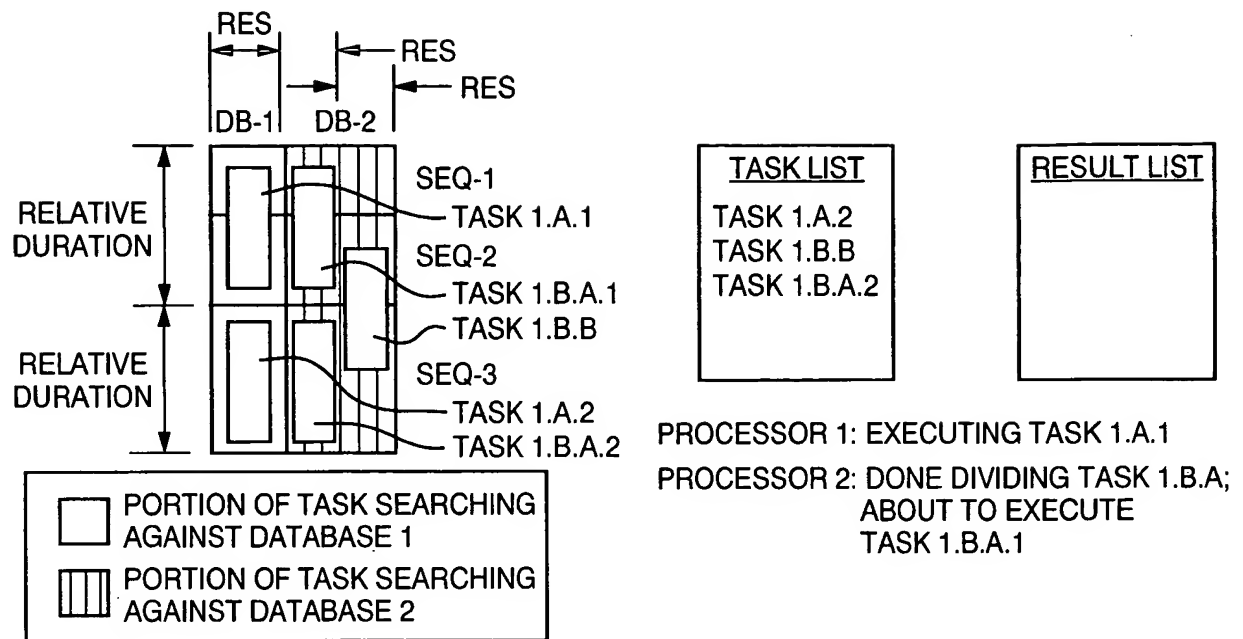


FIG. 3E

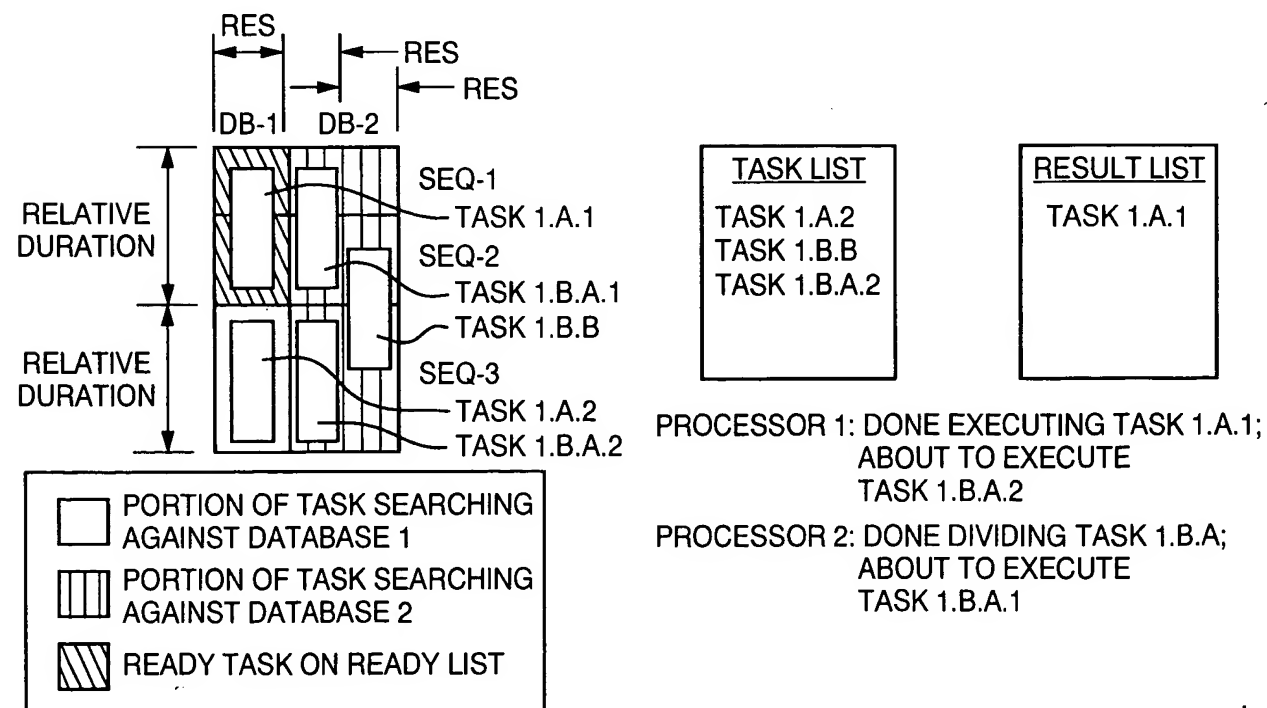


FIG. 3F

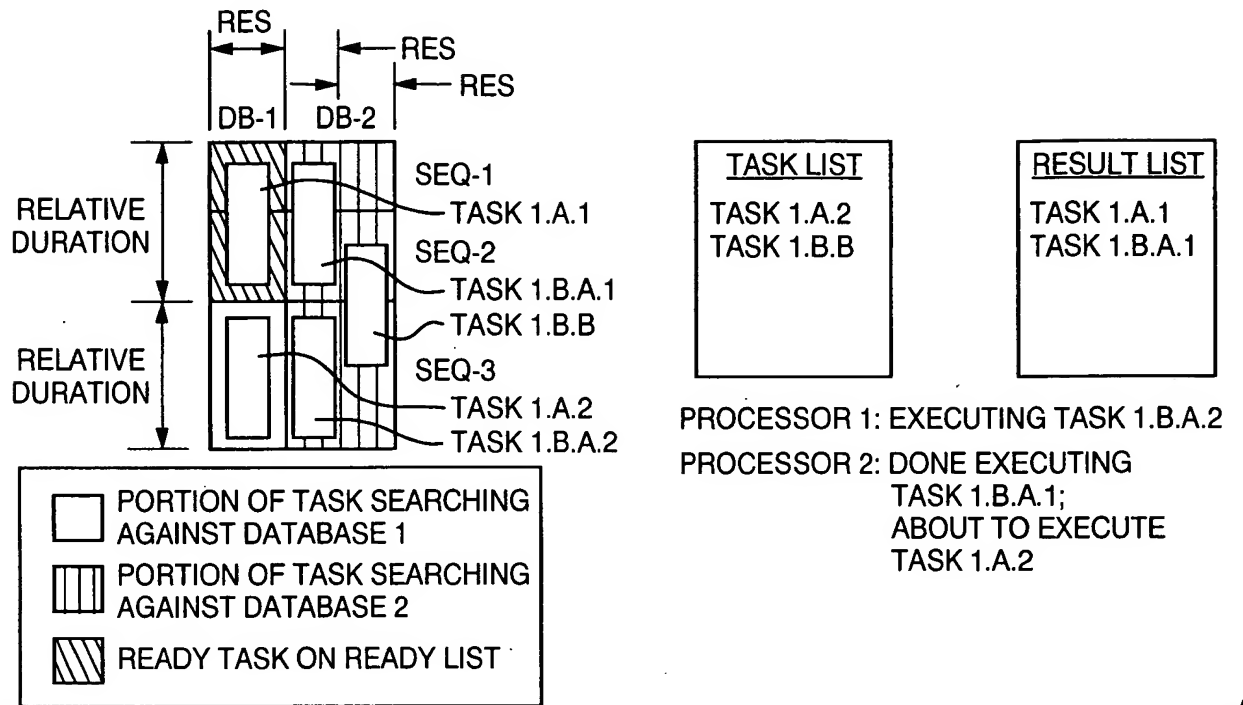


FIG. 3G

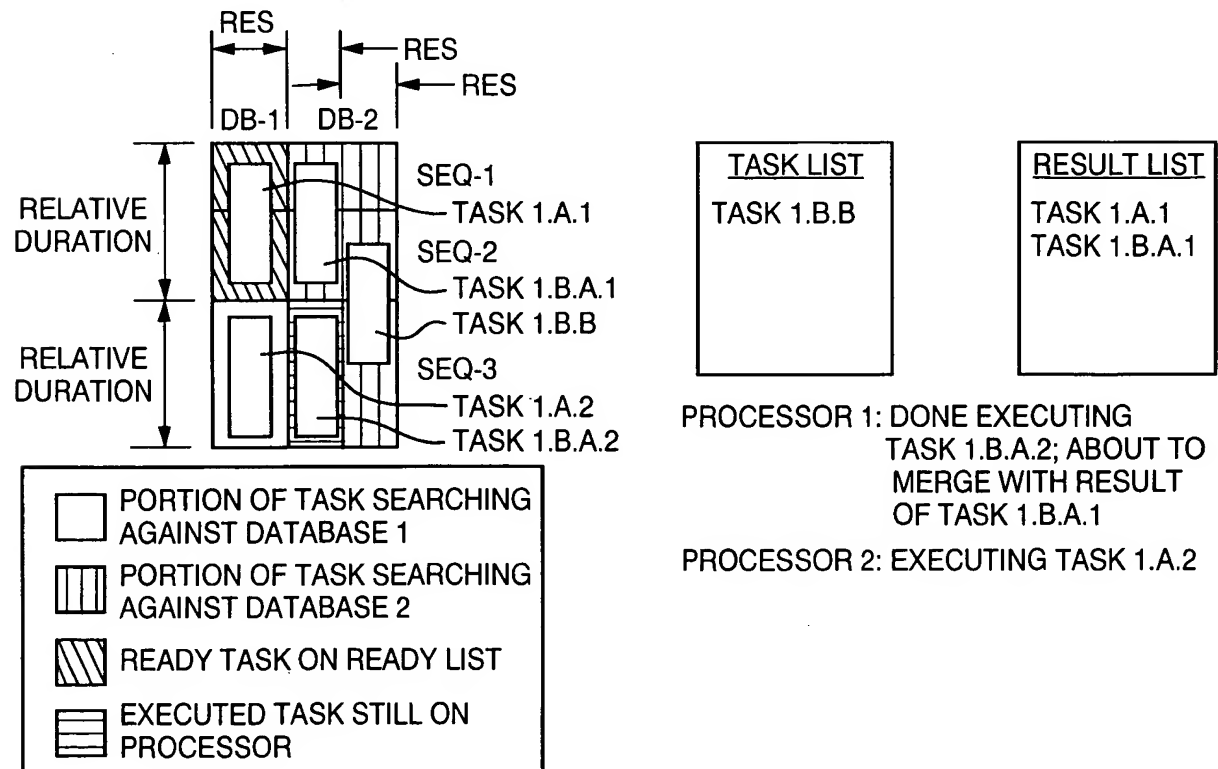


FIG. 3H

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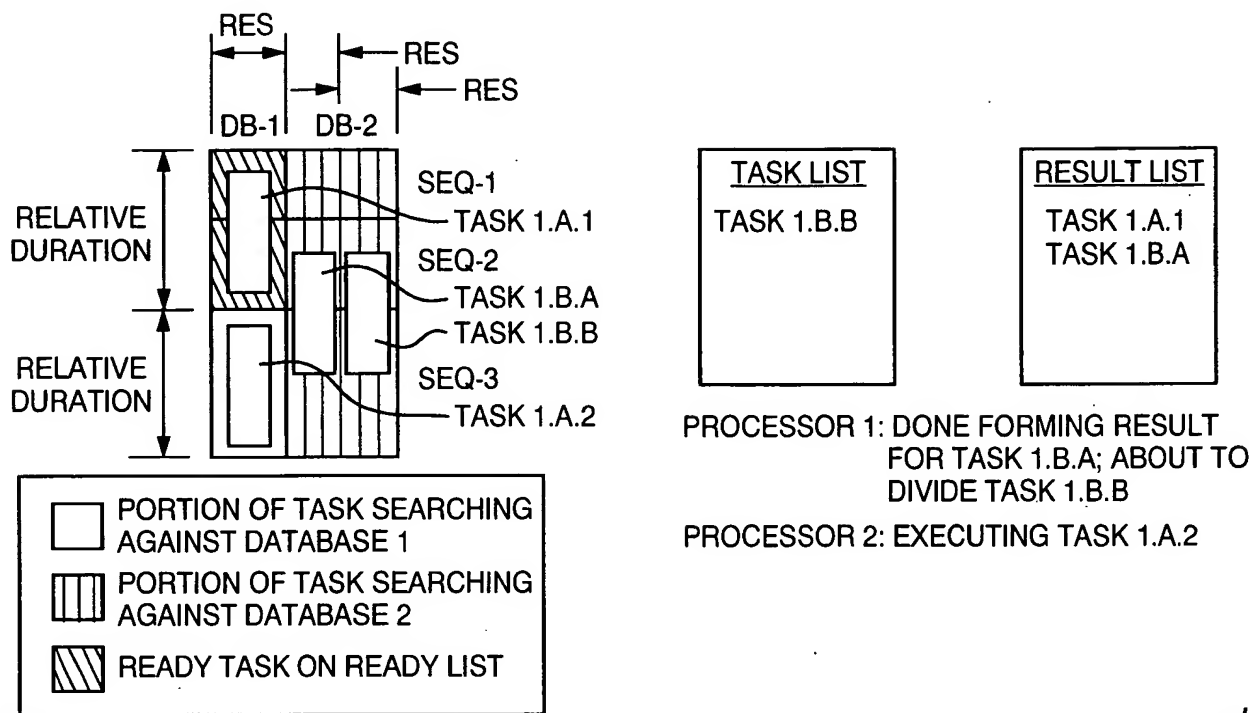


FIG. 3I

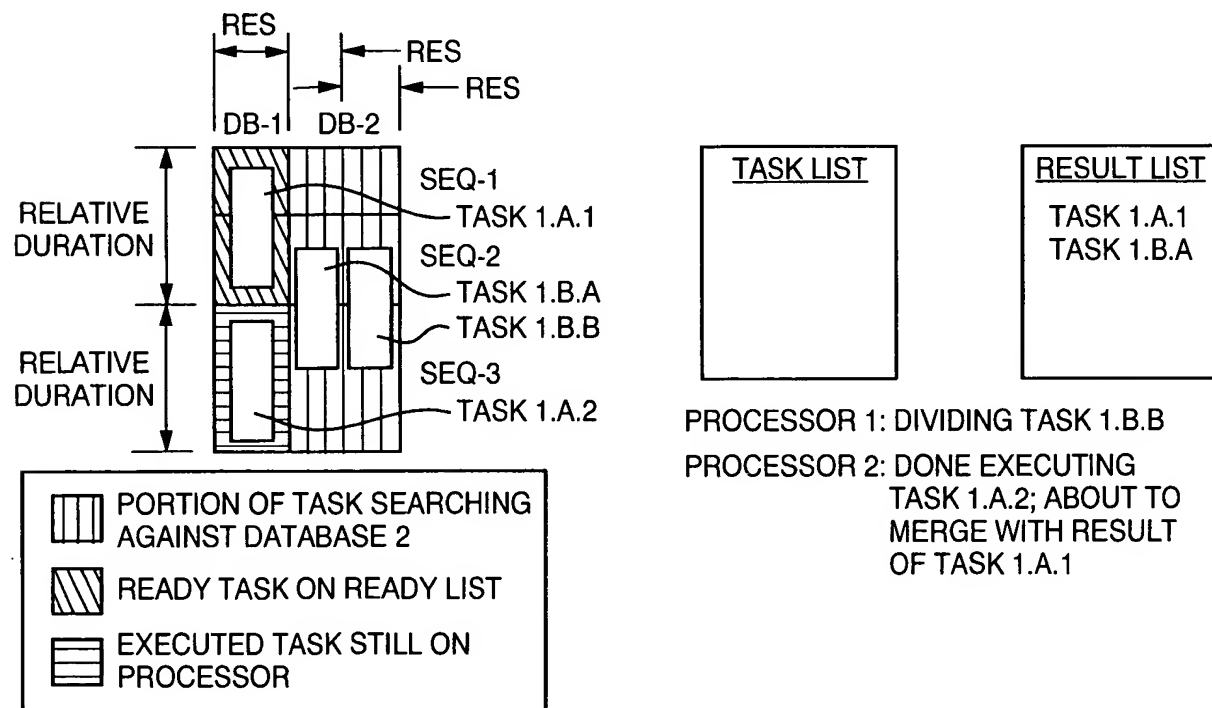


FIG. 3J

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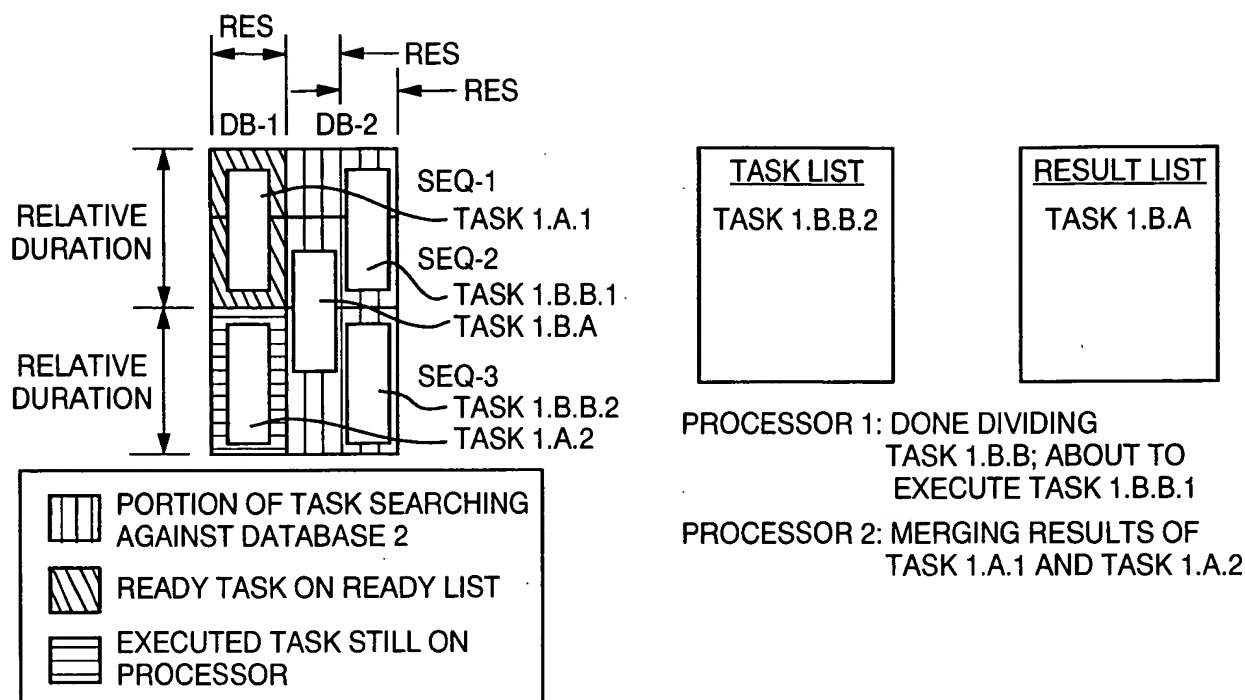


FIG. 3K

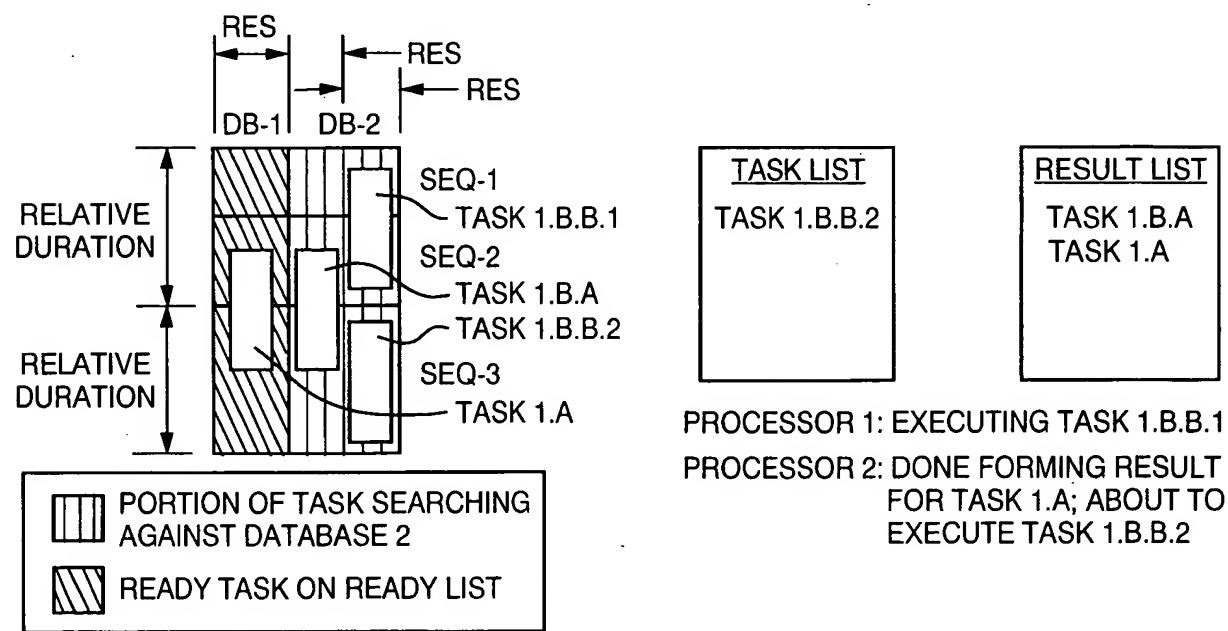


FIG. 3L



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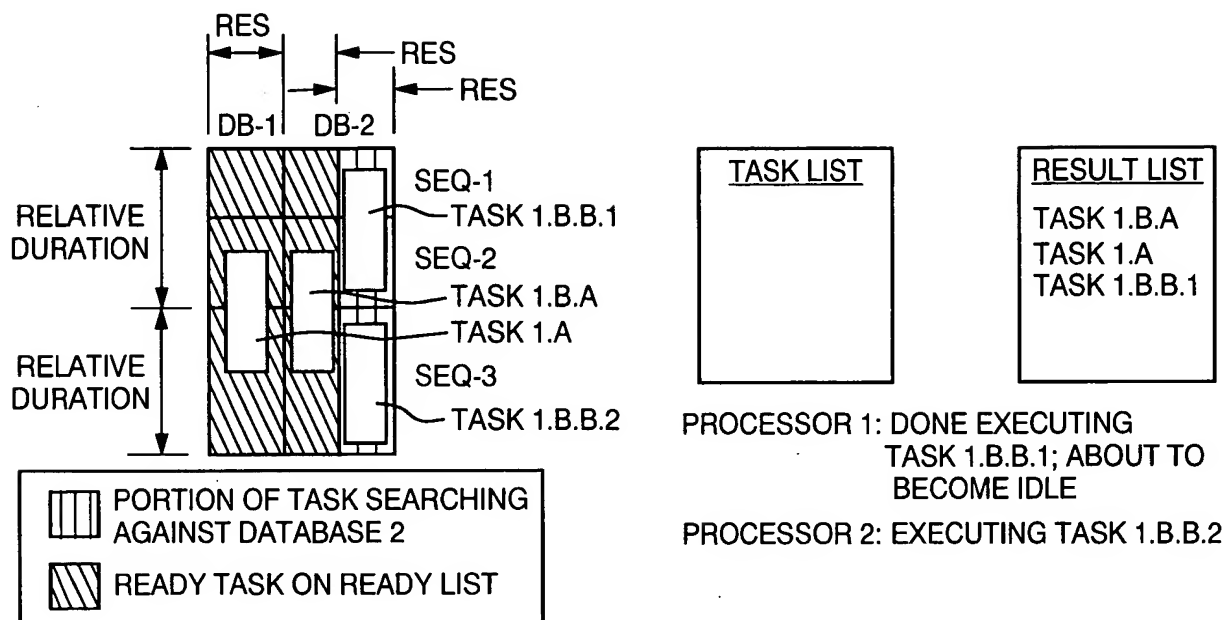


FIG. 3M

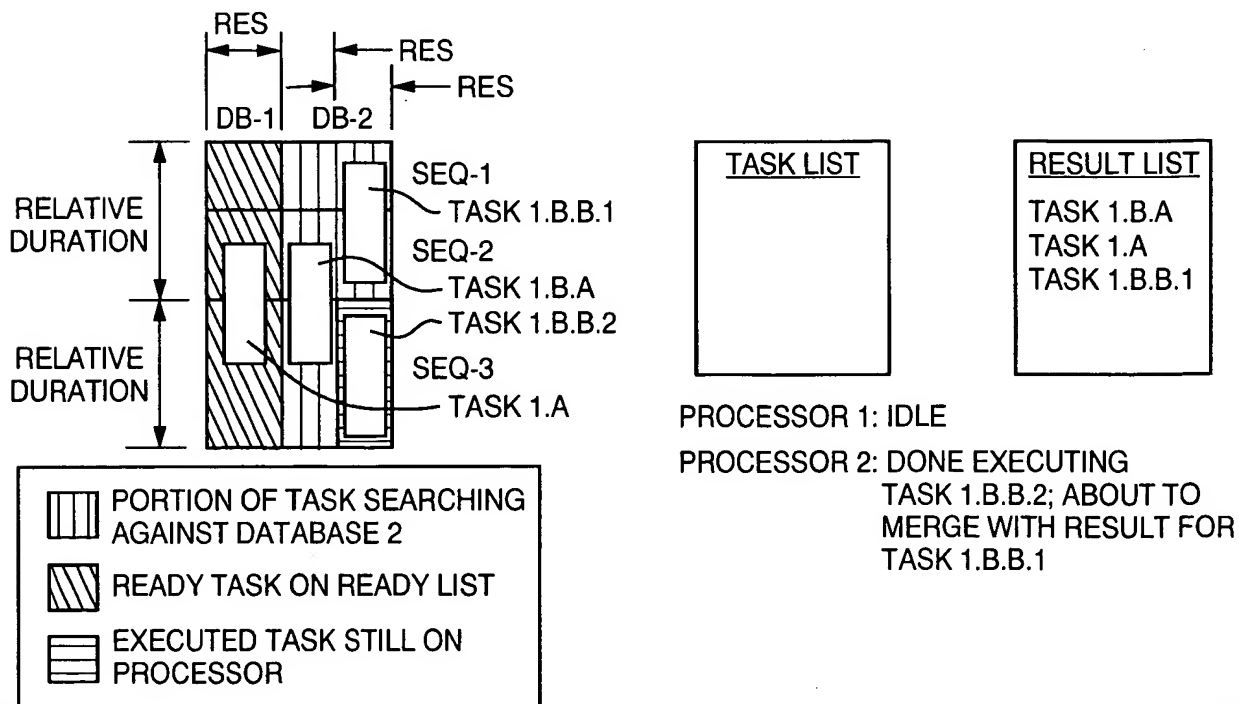


FIG. 3N

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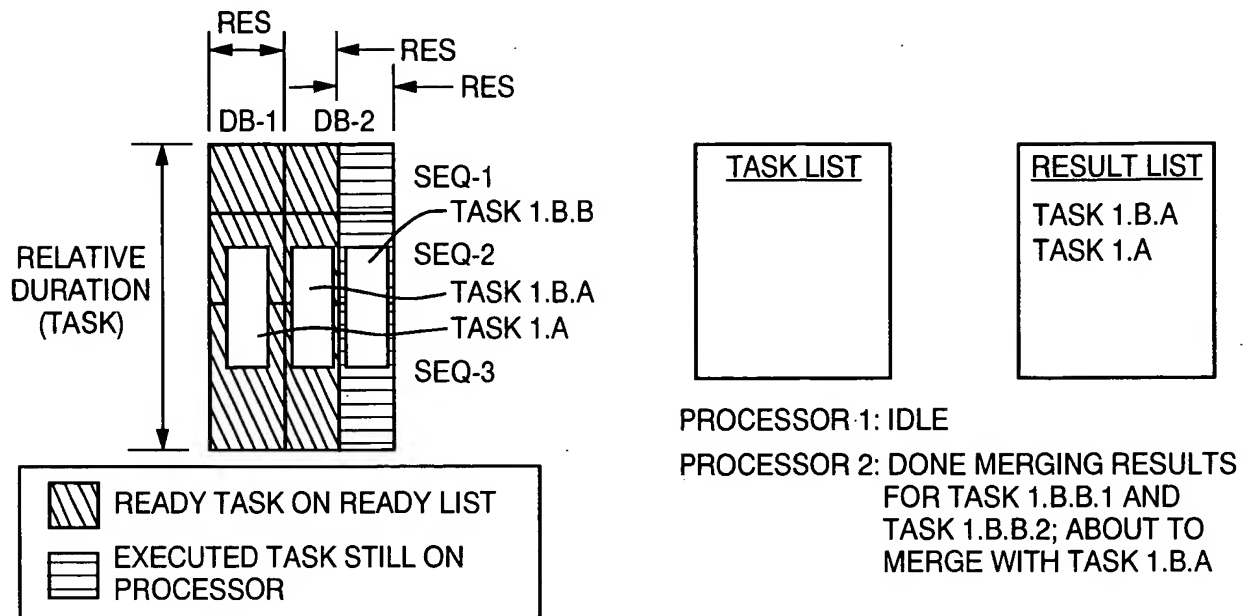


FIG. 30

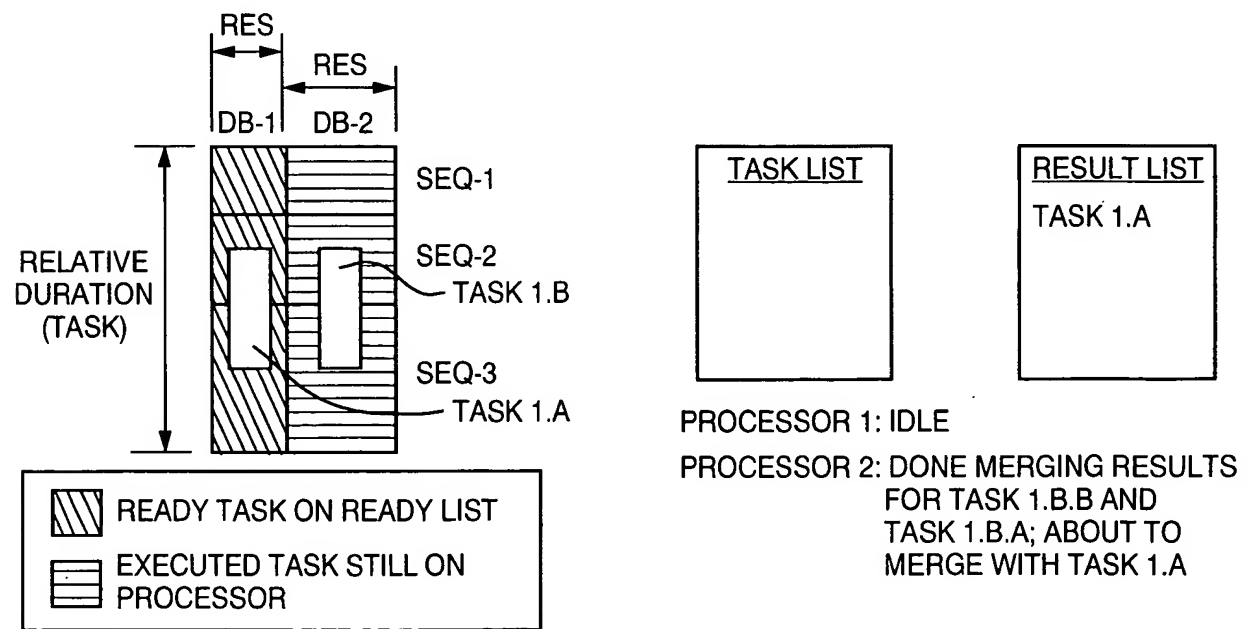


FIG. 3P

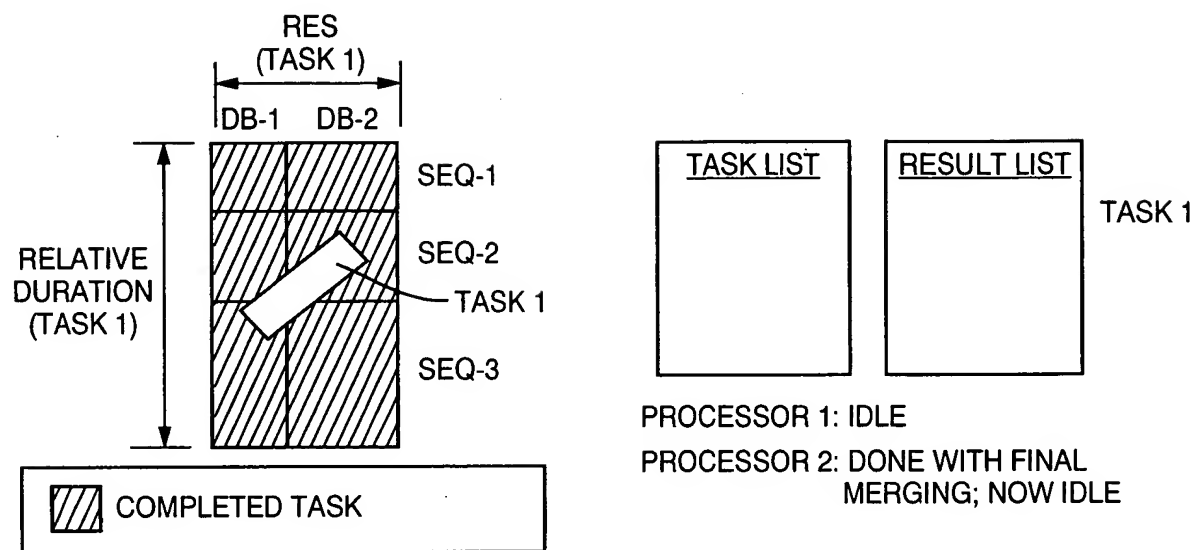


FIG. 3Q

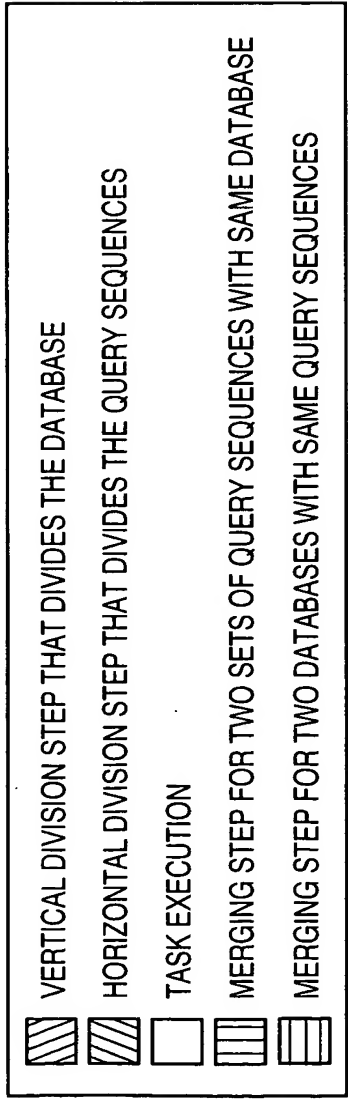
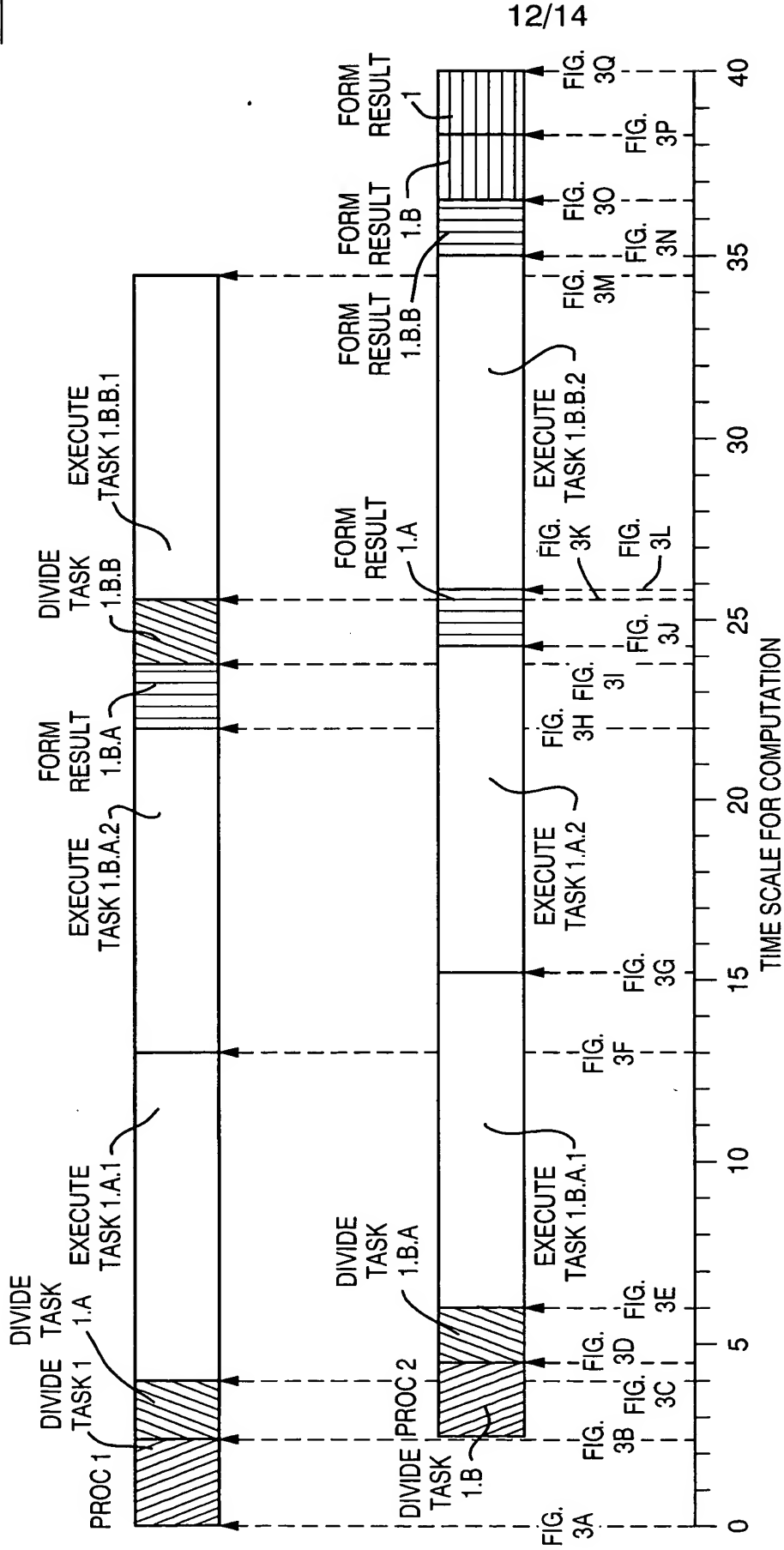


FIG. 4



FIG. 5



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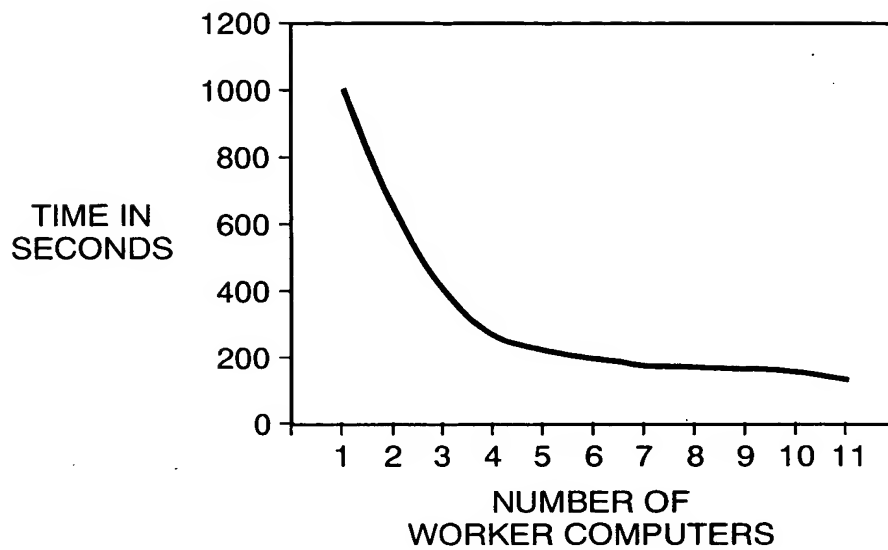


FIG. 6A

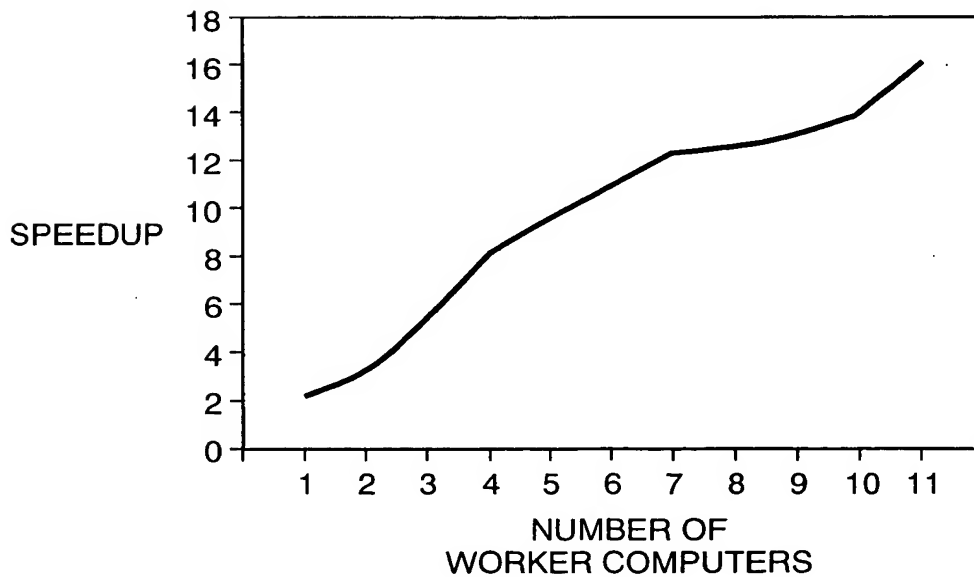


FIG. 6B

